CERTIFICATE

I, Tadashi UEDA, residing at 1994-152, Hazama-cho, Hachioji-shi Tokyo, 193-0941 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2003-74219 and certify that the following is a true translation to the best of my knowledge and belief.

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[Inventor]

[Address] c/o Seiko Epson Corporation, 3-5, Owa 3-chome, Suwa-shi, Nagano-ken

[Name] Akiyoshi AOYAGI

[Applicant for Patent]

[Id. No.] 000002369

[Name] Seiko Epson Corporation

[Agent]

[Id. No.] 100066980

[Patent Attorney]

[Name] Tetsuya MORI

[Sub-agent]

[Id. No.] 100075579

[Patent Attorney]

[Name] Yoshiaki NAITO

[Sub-agent]

[Id. No.] 100103850

[Patent Attorney]

[Name] Hidetetsu SAI

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[Name of Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE, ELECTRONIC DEVICE, ELECTRONIC APPARATUS, METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING ELECTRONIC DEVICE

[Claims]

[Claim 1] A semiconductor device, comprising:

a first carrier substrate;

a first semiconductor chip mounted face down on the first carrier substrate;

a second carrier substrate;

a second semiconductor chip mounted on the second carrier substrate;

protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip;

a sealant for sealing the second semiconductor chip; and

a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first semiconductor chip is exposed.

[Claim 2] The semiconductor device according to Claim 1,

wherein the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip.

[Claim 3] The semiconductor device according to Claim 1 or 2,

wherein the sealant is a mold resin.

[Claim 4] The semiconductor device according to Claim 1 or 2,

wherein the position of the sidewall of the sealant coincides with that of the sidewall of the second carrier substrate.

[Claim 5] The semiconductor device according to any one of Claims 1 to 4,

wherein the first semiconductor chip is connected to the first carrier substrate by pressure welding.

[Claim 6] The semiconductor device according to any one of Claims 1 to 5,

wherein, at the same temperature, the elastic modulus of a semiconductor device including the first carrier substrate and the first semiconductor chip mounted on the first carrier substrate is different from the elastic modulus of a semiconductor device including the second carrier substrate and the second semiconductor chip mounted on the second carrier substrate.

[Claim 7] The semiconductor device according to any one of Claims 1 to 6,

wherein the first carrier substrate on which the first semiconductor chip is mounted is a flip-chip-mounted ball grid array, and

wherein the second carrier substrate on which the second semiconductor chip is mounted is a mold-sealed ball grid array or a chip size package.

[Claim 8] The semiconductor device according to any one of Claims 1 to 7,

wherein the first semiconductor chip comprises a plurality of semiconductor chips mounted in parallel on the first carrier substrate.

[Claim 9] The semiconductor device according to any one of Claims 1 to 8,

wherein the second semiconductor chip comprises a plurality of stacked semiconductor chips.

[Claim 10] The semiconductor device according to any one of Claims 1 to 9,

wherein the second semiconductor chip comprises a plurality of semiconductor chips mounted in parallel on the second carrier substrate.

[Claim 11] A semiconductor device, comprising:

a carrier substrate;

a first semiconductor chip mounted face down on the carrier substrate;

a second semiconductor chip on which re-arrangement wiring line layers are formed on surfaces where electrode pads are formed; and

protruding electrodes for connecting the second semiconductor chip to the carrier substrate so that the second semiconductor chip is held above the first semiconductor chip.

[Claim 12] An electronic device, comprising:

a first carrier substrate;

a first electronic part mounted on the first carrier substrate;

a second carrier substrate;

a second electronic part mounted on the second carrier substrate;

protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first electronic part;

a sealant for sealing the second electronic part; and

a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first electronic part is exposed.

[Claim 13] An electronic apparatus, comprising:

a first carrier substrate;

a semiconductor chip mounted on the first carrier substrate;

a second carrier substrate;

a second semiconductor chip mounted on the second carrier substrate;

protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip;

a sealant for sealing the second semiconductor chip;

a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first semiconductor chip is exposed; and

a mother substrate on which the first carrier substrate is mounted.

[Claim 14] A method of manufacturing a semiconductor device, comprising the steps of:

mounting a first semiconductor chip face down on a first carrier substrate so that the reverse face of the first semiconductor chip is exposed;

mounting a second semiconductor chip on a second carrier substrate;

sealing the second semiconductor chip with a sealing resin; and

connecting the second carrier substrate to the first carrier substrate via protruding electrodes so that the second carrier substrate is held above the first semiconductor chip so as to be separated from the first semiconductor chip.

[Claim 15] The method of manufacturing a semiconductor device according to Claim 14,

wherein the step of sealing the second semiconductor chip with the sealing resin comprises the steps of:

integrally molding a plurality of the second semiconductor chips, which are mounted on the second carrier substrate, with the sealing resin; and

cutting the second carrier substrate molded with the sealing resin into pieces so that each piece includes one of the second semiconductor chips.

[Claim 16] A method of manufacturing an electronic device, comprising the steps of:

mounting a first electronic part on a first carrier substrate so that the reverse face of the first electronic part is exposed;

mounting a second electronic part on a second carrier substrate;

sealing the second electronic part with a sealing resin; and

connecting the second carrier substrate to the first carrier substrate via protruding electrodes so that the second carrier substrate is held above the first electronic part so as to be separated from the first electronic part.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device, an electronic device, an electronic apparatus, a method of manufacturing a semiconductor device, and a method of manufacturing an electronic device which are suitable for application to, in particular, a stacked structure of semiconductor packages.

[0002]

[Description of the Related Art]

In a conventional semiconductor device, in order to save space when semiconductor chips are mounted, for example, as disclosed in Japanese Patent Document 1, a method of three-dimensionally mounting semiconductor chips on a carrier substrate is used.

[0003]

[Patent Document 1]

Japanese Unexamined Patent Application Publication No. 10-284683

[0004]

[Problems to be Solved by the Invention]

However, in the method of three-dimensionally mounting semiconductor chips via a carrier substrate, it is difficult to stack different kinds of chips while allowing for heat dissipation.

Accordingly, an object of the present invention is to provide a semiconductor device, an electronic device, an electronic apparatus, a method of manufacturing a semiconductor device, and a method of manufacturing an electronic device which are capable of realizing a structure in which different kinds of chips can be three-

dimensionally mounted while ensuring good heat dissipation characteristics.

[0005]

[Means for Solving the Problems]

In order to achieve the above object, according to one aspect of the present invention, there is provided A semiconductor device, comprising: a first carrier substrate; a first semiconductor chip mounted face down on the first carrier substrate; a second carrier substrate; a second semiconductor chip mounted on the second carrier substrate; protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip; a sealant for sealing the second semiconductor chip; and a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first semiconductor chip is exposed.

[0006]

According to the above structure, it is possible to stack differently packaged second semiconductor chip on the first semiconductor chip in a state where the reverse face of the first semiconductor chip mounted face down on the first carrier substrate are exposed. As a result, even when the second carrier substrate is stacked on the first carrier substrate, it is possible to allow for proper heat dissipation from the first semiconductor chip and to realize a structure in which different kinds of chips are three-dimensionally mounted.

[0007]

Further, in a semiconductor device according to one aspect of the present invention, the second carrier substrate is fixed to the first carrier substrate so as to be mounted on the first semiconductor chip.

According to the above structure, it is possible to overlap the first semiconductor chip and the second semiconductor chip with each other. As a result, it is possible to

reduce mounting area when a plurality of semiconductor chips is mounted and thereby to save space when the semiconductor chips are mounted.

[0008]

Further, in a semiconductor device according to one aspect of the present invention, the sealant is a mold resin.

According to the above structure, it is possible to stack different kinds of packages including the second carrier substrate on the first carrier substrate and thereby to realize a structure in which the semiconductor chips are three-dimensionally mounted even when the kinds of the semiconductor chips vary.

[0009]

Further, in a semiconductor device according to one aspect of the present invention, the position of the sidewall of the sealant coincides with that of the sidewall of the second carrier substrate.

According to the above structure, it is possible to reinforce one entire surface of the second carrier substrate with a sealant for sealing the second semiconductor chip while suppressing an increase in the height when the second carrier substrate is stacked on the first carrier substrate and to seal the second semiconductor chip without dividing the sealant into cells. As a result, it is possible to increase the mounting area of the second semiconductor chip mounted on the second carrier substrate.

[0010]

Further, in a semiconductor device according to one aspect of the present invention, the first semiconductor chip is connected to the first carrier substrate by pressure welding.

According to the above structure, it is possible to lower the temperature when the first semiconductor chip is connected to the first carrier substrate and thereby to reduce the warpage of the first carrier substrate when the first carrier substrate is actually used.

[0011]

Further, in a semiconductor device according to one aspect of the present invention, the elastic modulus of a semiconductor device including the first carrier substrate and the first semiconductor chip mounted on the first carrier substrate is different from the elastic modulus of a semiconductor device including the second carrier substrate and the second semiconductor chip mounted on the second carrier substrate at the same temperature.

According to the above structure, it is possible to prevent the warpage of one carrier substrate by the other carrier substrate and thereby to improve connection reliability between the first carrier substrate and the second carrier substrate.

[0012]

Further, in a semiconductor device according to one aspect of the present invention, the first carrier substrate on which the first semiconductor chip is mounted is a flip-chip-mounted ball grid array, and the second carrier substrate on which the second semiconductor chip is mounted is a mold-sealed ball grid array or a chip size package.

According to the above structure, it is possible to stack different kinds of packages while suppressing an increase in the height of a structure in which the semiconductor chips are three-dimensionally mounted and thereby to save space when the semiconductor chips are mounted even when the kinds of the semiconductor chips vary.

[0013]

Further, in a semiconductor device according to one aspect of the present invention, the first semiconductor chip comprises a plurality of semiconductor chips mounted in parallel on the first carrier substrate.

According to the above structure, it is possible to overlap the second semiconductor chip and the plurality of first semiconductor chips with each other and thereby to reduce the mounting area when the plurality of semiconductor chips is mounted. As a result, it is

possible to save space when the semiconductor chips are mounted.

[0014]

Further, in a semiconductor device according to one aspect of the present invention, the second semiconductor chip comprises a plurality of stacked semiconductor chips.

According to the above structure, it is possible to stack a plurality of second semiconductor chips having different kinds and sizes on the first semiconductor chips and thereby to save space when the semiconductor chips are mounted, and it is possible to let the semiconductor chips have various functions.

[0015]

Further, in a semiconductor device according to one aspect of the present invention, the second semiconductor chip comprises a plurality of semiconductor chips mounted in parallel on the second carrier substrate.

According to the above structure, it is possible to arrange the plurality of second semiconductor chips on the first semiconductor chips while suppressing an increase in the height when the second semiconductor chips are stacked. As a result, it is possible to suppress the deterioration of connection reliability when the semiconductor chips are three-dimensionally mounted and to save space when the semiconductor chips are mounted.

[0016]

Further, according to one aspect of the present invention, there is provided a semiconductor device, comprising: a carrier substrate; a first semiconductor chip mounted face down on the carrier substrate; a second semiconductor chip on which re-arrangement wiring line layers are formed on surfaces where electrode pads are formed; and protruding electrodes for connecting the second semiconductor chip to the carrier substrate so that the second semiconductor chip is held above the first semiconductor chip.

[0017]

According to the above structure, even when the kinds or the sizes of the semiconductor chips vary, it is possible to flip-chip mount the second semiconductor chip on the carrier substrate so that the second semiconductor chip are arranged on the first semiconductor chip in a state where the reverse face of the first semiconductor chip is exposed without interposing the carrier substrates between the first semiconductor chip and the second semiconductor chip.

[0018]

For this reason, it is possible to allow for proper heat dissipation while suppressing an increase in the height when the semiconductor chips are stacked and thereby to save space when the semiconductor chips are mounted while suppressing the deterioration of the reliability of the three-dimensionally mounted semiconductor chips.

Further, according to one aspect of the present invention, there is provided an electronic device, comprising: a first carrier substrate; a first electronic part mounted on the first carrier substrate; a second carrier substrate; a second electronic part mounted on the second carrier substrate; protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first electronic part; a sealant for sealing the second electronic part; and a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first electronic part is exposed.

[0019]

According to the above structure, it is possible to stack the differently packaged second electronic parts on the first electronic parts in a state where the reverse face of the first electronic part mounted face down on the first carrier substrate are exposed. As a result, even when the second carrier substrate is stacked on the first carrier substrate, it is

possible to allow for proper heat dissipation from the first electronic part and to realize a structure in which different kinds of parts are three-dimensionally mounted.

[0020]

Further, according to one aspect of the present invention, there is provided an electronic apparatus, comprising: a first carrier substrate; a semiconductor chip mounted on the first carrier substrate; a second carrier substrate; a second semiconductor chip mounted on the second carrier substrate; protruding electrodes for connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip; a sealant for sealing the second semiconductor chip; a resin provided between the first carrier substrate and the second carrier substrate so that the reverse face of the first semiconductor chip is exposed; and a mother substrate on which the first carrier substrate is mounted.

[0021]

According to the above structure, it is possible to stack the differently packaged second semiconductor chip on the first semiconductor chip in a state where the reverse face of the first semiconductor chip mounted face down on the first carrier substrate are exposed. As a result, it is possible to realize a structure in which different kinds of chips are three-dimensionally mounted while allowing for proper heat dissipation from the first semiconductor chip.

Further, according to one aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising the steps of: mounting a first semiconductor chip face down on a first carrier substrate so that the reverse face of the first semiconductor chip is exposed; mounting a second semiconductor chip on a second carrier substrate; sealing the second semiconductor chip with a sealing resin; and connecting the second carrier substrate to the first carrier substrate via protruding

electrodes so that the second carrier substrate is held above the first semiconductor chip so as to be separated from the first semiconductor chip.

[0022]

According to the above structure, even when the second carrier substrate is stacked on the first carrier substrate, it is possible to expose the reverse face of the first semiconductor chip mounted face down on the first carrier substrate. Therefore, it is possible to effectively take out the heat generated by the first semiconductor chip and to stack the differently packaged second semiconductor chip on the first semiconductor chip. As a result, it is possible to realize a structure in which different kinds of chips are three-dimensionally mounted while allowing for proper heat dissipation.

[0023]

According to the above structure, in a method of manufacturing a semiconductor device according to one aspect of the present invention, the step of sealing the second semiconductor chip with the sealing resin comprises the steps of: integrally molding a plurality of the second semiconductor chips, which are mounted on the second carrier substrate, with the sealing resin; and cutting the second carrier substrate molded with the sealing resin into pieces so that each piece includes one of the second semiconductor chips.

[0024]

According to the above structure, it is possible to seal the second semiconductor chips with sealing resin without dividing the sealing resin into cells in each second semiconductor chip and to reinforce one entire surface of the second carrier substrate with the sealing resin.

For this reason, even when the kinds or the sizes of the second semiconductor chips vary, it is possible to share a mold when the second semiconductor chips are molded and thereby to make the sealing resin process efficient. Also, since space for dividing the

sealing resin into cells is unnecessary, it is possible to increase the mounting area of the semiconductor chips mounted on the second carrier substrate.

[0025]

Further, according to one aspect of the present invention, there is provided a method of manufacturing an electronic device, comprising the steps of: mounting a first electronic part on a first carrier substrate so that the reverse face of the first electronic part is exposed; mounting a second electronic part on a second carrier substrate; sealing the second electronic part with a sealing resin; and connecting the second carrier substrate to the first carrier substrate via protruding electrodes so that the second carrier substrate is held above the first electronic part so as to be separated from the first electronic part.

[0026]

According to the above structure, even when the second carrier substrate is stacked on the first carrier substrate, it is possible to expose the reverse face of the first electronic part mounted face down on the first carrier substrate. Therefore, it is possible to effectively take out the heat generated by the first electronic part and to stack the differently packaged second electronic part on the first electronic part. As a result, it is possible to allow for proper heat dissipation and to realize a structure in which different kinds of parts are three-dimensionally mounted.

[0027]

[Description of the Embodiments]

A semiconductor device and an electronic device and a method of manufacturing the same according to the embodiments of the present invention will now be described with reference to the drawings.

Fig. 1 is a sectional view illustrating the structure of a semiconductor device according to a first embodiment of the present invention. According to the first

embodiment, a semiconductor package PK12 in which stacked semiconductor chips (or semiconductor dies) 33a and 33b are wire-bonded to a carrier substrate 31 is stacked on a semiconductor package PK11 in which a semiconductor chip (or a semiconductor die) 23 is mounted on a carrier substrate 21 by anisotropic conductive film (ACF) bonding.

[0028]

In Fig. 1, a carrier substrate 21 is provided in the semiconductor package PK11. Lands 22a and 22c are respectively formed on both faces of the carrier substrate 21. Internal wiring lines 22b are formed in the carrier substrate 21. A semiconductor chip 23 is flip-chip mounted on the carrier substrate 21 so that the reverse face of the semiconductor chip 23 is exposed. Protruding electrodes 24 for flip-chip mounting the semiconductor chip 23 are provided on the semiconductor chip 23. The protruding electrodes 24 provided on the semiconductor chip 23 are bonded to the lands 22c via an anisotropic conductive film 25 by ACF bonding. Further, protruding electrodes 26 for mounting the carrier substrate 21 on a mother substrate are provided on the lands 22a on the reverse face of the carrier substrate 21.

[0029]

Since the semiconductor chip 23 is mounted on the carrier substrate 21 by ACF bonding, space for performing wire bonding or mold sealing is unnecessary. Therefore, it is possible to save space when the semiconductor chips are three-dimensionally mounted and to lower the temperature when the semiconductor chip 23 is bonded to the carrier substrate 21. As a result, it is possible to reduce the warpage of the carrier substrate 21 when the carrier substrate 21 is actually used.

[0030]

On the other hand, a carrier substrate 31 is provided in the semiconductor package PK12. Lands 32a and 32c are respectively formed on both faces of the carrier substrate 31.

Internal wiring lines 32b are formed in the carrier substrate 31. A semiconductor chip 33a is mounted face up on the carrier substrate 31 via an adhesion layer 34a. The semiconductor chip 33a is wire-bonded to the lands 32c via conductive wires 35a. Furthermore, a semiconductor chip 33b is mounted face up on the semiconductor chip 33a so as to avoid the conductive wires 35a. The semiconductor chip 33b is fixed to the semiconductor chip 33a via an adhesion layer 34b and is wire-bonded to the lands 32c via conductive wires 35b.

[0031]

Further, protruding electrodes 36 for mounting the carrier substrate 31 on the carrier substrate 21 are provided on the lands 32a on the reverse face of the carrier substrate 31 so that the carrier substrate 31 is held above the semiconductor chip 23 so as to be separated from the semiconductor chip 23. The protruding electrodes 36 are arranged so as to avoid the region on which the semiconductor chip 23 is mounted. It is possible to arrange the protruding electrodes 36, for example, around a peripheral region of the reverse face of the carrier substrate 31. The carrier substrate 31 is mounted on the carrier substrate 21 in a state where the reverse face of the semiconductor chip 23 is exposed by bonding the protruding electrodes 36 to the lands 22c provided on the carrier substrate 21.

[0032]

Thus, it is possible to stack the differently packaged semiconductor chips 33a and 33b on the semiconductor chip 23 in a state where the reverse face of the semiconductor chip 23 mounted face down on the carrier substrate 21 is exposed. As a result, even when the carrier substrate 31 is stacked on the carrier substrate 21, it is possible to allow for proper heat dissipation from the semiconductor chip 23 and to realize a structure in which different kinds of semiconductor chips 23, 33a, and 33b are three-dimensionally mounted.

[0033]

Further, the semiconductor chips 33a and 33b are sealed with a sealing resin 37. The sealing resin 37 can be molded using a thermosetting resin such as epoxy resin.

The sealing resin 37 is molded on one entire surface of the carrier substrate 31 on which the semiconductor chips 33a and 33b are mounted. Therefore, even when the various kinds of semiconductor chips 33a and 33b are mounted on the carrier substrate 31, it is possible to share a mold when the sealing resin 37 is molded and thereby to make the sealing resin process efficient. Also, since space for dividing the sealing resin 37 into cells is unnecessary, it is possible to increase the mounting area of the semiconductor chips 33a and 33b mounted on the carrier substrate 31.

[0034]

For example, a dual-sided substrate, a multi-layer wiring line substrate, a built-up substrate, a tape substrate or a film substrate may be used as the carrier substrates 21 and 31. The carrier substrates 21 and 31 may be made of, for example, polyimide resin, glass epoxy resin, BT resin, a composite of aramide and epoxy, and ceramic. For example, an Au bump, a Cu bump and a Ni bump coated with solder, and solder balls may be used as the protruding electrodes 24, 26, and 36. Since solder balls are used as the protruding electrodes 26 and 36, it is possible to stack the different kinds of packages PK11 and PK12 on each other by using regular BGA and thereby to apply the manufacturing line to other fields. For example, Au wire and Al wire can be used as the conductive wires 35a and 35b. A method of providing the protruding electrodes 36 on the lands 32a of the carrier substrate 31 in order to mount the carrier substrate 31 on the carrier substrate 21 is described in the above-mentioned embodiment. However, the protruding electrodes 36 may be provided on the lands 22c of the carrier substrate 21.

[0035]

Further, a method of mounting the semiconductor chip 23 on the carrier substrate 21 by ACF bonding is described in the above-mentioned embodiment. However, for example, pressure welding such as nonconductive film (NCF) bonding, anisotropic conductive paste (ACP) bonding, or nonconductive paste (NCP) bonding may be used. Metal joining such as soldering or alloy joining may be used. Furthermore, a method of mounting only one semiconductor chip 23 on the carrier substrate 21 is described in the above-mentioned embodiment. However, a plurality of semiconductor chips may also be mounted on the carrier substrate 21.

[0036]

Fig. 2 is a sectional view illustrating the structure of a semiconductor device according to a second embodiment of the present invention. According to the second embodiment, a semiconductor package PK22 in which stacked semiconductor chips 53a and 53b are flip-chip mounted and wire-bonded, respectively, is stacked on a semiconductor package PK21 in which a semiconductor chip 43 is mounted by ACF bonding.

[0037]

In Fig. 2, a carrier substrate 41 is provided in the semiconductor package PK21. Lands 42a and 42c are respectively formed on both faces of the carrier substrate 41. Internal wiring lines 42b are formed in the carrier substrate 41. The semiconductor chip 43 is flip-chip mounted on the carrier substrate 41 so that the reverse face thereof is exposed. Protruding electrodes 44 for flip-chip mounting the semiconductor chip 43 are provided on the semiconductor chip 43. The protruding electrodes 44 provided on the semiconductor chip 43 are bonded to the lands 42c via an anisotropic conductive film 45 by ACF bonding. Protruding electrodes 46 for mounting the carrier substrate 41 on a mother substrate are provided on the lands 42a the reverse face of the carrier substrate 41.

[0038]

Since the semiconductor chip 43 is mounted on the carrier substrate 41 by ACF bonding, a space for performing wire bonding or mold sealing is unnecessary. Therefore, it is possible to save space when the semiconductor chip 43 is three-dimensionally mounted and to lower the temperature when the semiconductor chip 43 is bonded to the carrier substrate 41. As a result, it is possible to reduce the warpage of the carrier substrate 41 when the carrier substrate 41 is actually used.

[0039]

On the other hand, a carrier substrate 51 is provided in the semiconductor package PK22. Lands 52a and 52c are respectively formed on both faces of the carrier substrate 51. Internal wiring lines 52b are formed in the carrier substrate 51. A semiconductor chip 53a is flip-chip mounted on the carrier substrate 51. Protruding electrodes 55a for flip-chip mounting the semiconductor chip 53a are provided on the semiconductor chip 53a. The protruding electrodes 55a provided on the semiconductor chip 53a are bonded to the lands 52a via an anisotropic conductive film 54a by ACF bonding. Furthermore, a semiconductor chip 53b is mounted face up on the semiconductor chip 53a. The semiconductor chip 53b is fixed to the semiconductor chip 53a via an adhesion layer 54b and is wire-bonded to the lands 52c via conductive wires 55b.

[0040]

It is possible to stack the semiconductor chip 53b of a size equal to or larger than the semiconductor chip 53a on the semiconductor chip 53a by mounting the semiconductor chip 53b face up on the face-down mounted semiconductor chip 53a without interposing the carrier substrate and thereby to reduce the mounting area.

[0041]

Further, protruding electrodes 56 for mounting the carrier substrate 51 on the

carrier substrate 41 are provided on the lands 52a on the reverse face of the carrier substrate 51 so that the carrier substrate 51 is held above the semiconductor chip 43 so as to be separated from the semiconductor chip 43. The protruding electrodes 56 are arranged so as to avoid the region on which the semiconductor chip 43 is mounted. It is possible to arrange the protruding electrodes 56, for example, around a peripheral region of the reverse face of the carrier substrate 51. The carrier substrate 51 is mounted on the carrier substrate 41 in a state where the reverse face of the semiconductor chip 43 is exposed by bonding the protruding electrodes 56 to the lands 42c provided on the carrier substrate 41.

[0042]

Thus, it is possible to stack the differently packaged semiconductor chips 53a and 53b on the semiconductor chip 43 in a state where the reverse face of the semiconductor chip 43 mounted face down on the carrier substrate 41 is exposed. As a result, even when the carrier substrate 51 is stacked on the carrier substrate 41, it is possible to allow for proper heat dissipation from the semiconductor chip 43 and to realize a structure in which different kinds of semiconductor chips 43, 53a, and 53b are three-dimensionally mounted.

[0043]

For example, solder balls may be used as the protruding electrodes 46 and 56. Therefore, it is possible to stack the different kinds of packages PK21 and PK22 on each other by using regular BGA and thereby to apply the manufacturing line to other fields.

Further, the semiconductor chips 53a and 53b are sealed with a sealing resin 57. The sealing resin 57 may be molded using a thermosetting resin such as epoxy resin.

[0044]

The sealing resin 57 is molded on one entire surface of the carrier substrate 51 on which the semiconductor chips 53a and 53b are mounted. Therefore, even when the

various kinds of semiconductor chips 53a and 53b are mounted on the carrier substrate 51, it is possible to share a mold when the sealing resin 57 is molded and thereby to make the sealing resin process efficient. Also, since space for dividing the sealing resin 57 into cells is unnecessary, it is possible to increase the mounting area of the semiconductor chips 53a and 53b mounted on the carrier substrate 51.

[0045]

Fig. 3 is a sectional view illustrating a method of manufacturing a semiconductor device according to a third embodiment of the present invention. According to the third embodiment, after a plurality of semiconductor chips 62a to 62c are integrally molded with a sealing resin 64, a carrier substrate 61 and the sealing resin 64 are cut into pieces so that each piece includes one of the semiconductor chips 62a to 62c. Therefore, sealing resins 64a to 64c are respectively formed on one entire surface of carrier substrates 61a to 61c on which the semiconductor chips 62a to 62c are respectively mounted.

[0046]

In Fig. 3(a), a mounting region on which the plurality of semiconductor chips 62a to 62c is mounted is provided in the carrier substrate 61. The plurality of semiconductor chips 62a to 62c is mounted on the carrier substrate 61 and is wire-bonded to the carrier substrate 61 via conductive wires 63a to 63c. Other than the method of wire-bonding the semiconductor chips 62a to 62c to the carrier substrate 61, the semiconductor chips 62a to 62c may be flip-chip mounted on the carrier substrate 61, and a structure in which the semiconductor chips 62a to 62c are stacked may be mounted on the carrier substrate 61.

[0047]

Next, as illustrated in Fig. 3(b), the plurality of semiconductor chips 62a to 62c mounted on the carrier substrate 61 are integrally molded with a sealing resin 64. Even when the various kinds of semiconductor chips 62a to 62c are mounted on the carrier

substrate 61 by integrally molding the plurality of semiconductor chips 62a to 62c with the sealing resin 64, it is possible to share a mold when the semiconductor chips 62a to 62c are molded and thereby to make the sealing resin process efficient. Also, since space for dividing the sealing resin 64 into cells is unnecessary, it is possible to increase the mounting area of the semiconductor chips 62a to 62c mounted on the carrier substrate 61.

[0048]

Next, as illustrated in Fig. 3(c), protruding electrodes 65a to 65c made of solder balls are respectively formed on the reverse faces of the carrier substrates 61a to 61c. As illustrated in Fig. 3(d), by cutting the carrier substrate 61 and the sealing resin 64 so that each cut piece includes one of the semiconductor chips 62a to 62c, the carrier substrate 61 is divided into the carrier substrates 61a to 61c on which the semiconductor chips 62a to 62c are respectively sealed with the sealing resins 64a to 64c. After cutting the carrier substrate 61 and the sealing resin 64 into pieces so that each cut piece includes one of the semiconductor chips 62a to 62c, the protruding electrodes made of solder balls may be formed.

[0049]

It is possible to respectively form the sealing resins 64a to 64c on one entire surface of the carrier substrates 61a to 61c on which the semiconductor chips 62a to 62c are mounted by integrally cutting the carrier substrate 61 and the sealing resin 64. Therefore, it is possible to improve the rigidity of the region in which the protruding electrodes 65a to 65c are arranged while preventing the manufacturing process from becoming complicated and thereby to reduce the warpage of the carrier substrates 61a to 61c.

[0050]

Fig. 4 is a sectional view illustrating a method of manufacturing a semiconductor device according to a fourth embodiment of the present invention. According to the fourth

embodiment, a semiconductor package PK32 sealed with a sealing resin 84 is stacked on a semiconductor package PK31 on which a semiconductor chip 73 is mounted by ACF bonding.

In Fig. 4(a), a carrier substrate 71 is provided in the semiconductor package PK31. Lands 72a and 72b are respectively formed on both faces of the carrier substrate 71. The semiconductor chip 73 is flip-chip mounted on the carrier substrate 71. Protruding electrodes 74 for flip-chip mounting the semiconductor chip 73 are provided on the semiconductor chip 73. The protruding electrodes 74 provided on the semiconductor chip 73 are bonded to the lands 72b via an anisotropic conductive film 75 by ACF bonding.

[0051]

On the other hand, a carrier substrate 81 is provided in a semiconductor package PK32. Lands 82 are formed on the reverse face of the carrier substrate 81. Protruding electrodes 83 made of solder balls are provided on the lands 82. Further, a semiconductor chip is mounted on the carrier substrate 81. One entire surface of the carrier substrate 81 on which the semiconductor chip is mounted is sealed with a sealing resin 84. A wire-bonded semiconductor chip may be mounted on the carrier substrate 81. A semiconductor chip may be flip-chip mounted on the carrier substrate 81. A structure in which semiconductor chips are stacked may be mounted on the carrier substrate 81.

[0052]

When the semiconductor package PK32 is stacked on the semiconductor package PK31, flux 76 is provided on the lands 72b of the carrier substrate 71. Soldering paste instead of the flux 76 may be provided on the lands 72b of the carrier substrate 71.

Next, as illustrated in Fig. 4(b), protruding electrodes 83 are bonded to the lands 72b by mounting the semiconductor package PK32 on the semiconductor package PK31 and performing a reflow process.

[0053]

Next, as illustrated in Fig. 4(c), protruding electrodes 77 for mounting the carrier substrate 71 on the lands 72a on the reverse face of the carrier substrate 71 on a mother substrate are formed.

Fig. 5 is a sectional view illustrating the structure of a semiconductor device according to a fifth embodiment of the present invention. According to the fifth embodiment, a structure in which semiconductor chips 113a to 113c are stacked is three-dimensionally mounted on a carrier substrate 101 on which a semiconductor chip 103 is flip-chip mounted.

[0054]

In Fig. 5, the carrier substrate 101 is provided in a semiconductor package PK41. Lands 102a and 102c are respectively formed on both faces of the carrier substrate 101. Internal wiring lines 102b are formed in the carrier substrate 101. The semiconductor chip 103 is flip-chip mounted on the carrier substrate 101 so that the reverse face of the semiconductor chip 103 is exposed. Protruding electrodes 104 for flip-chip mounting the semiconductor chip 103 are provided on the semiconductor chip 103. The protruding electrodes 104 provided on the semiconductor chip 103 are bonded to the lands 102c via an anisotropic conductive film 105 by ACF bonding. When the semiconductor chip 103 is mounted on the carrier substrate 101, alternatives to ACF bonding may be used; for example, pressure welding such as NCF bonding, NCP bonding, and ACP bonding may be used. Metal joining such as soldering and alloy joining may be used. Protruding electrodes 106 for mounting the carrier substrate 101 on a mother substrate are provided on the lands 102a provided on the reverse face of the carrier substrate 101.

[0055]

On the other hand, a carrier substrate 111 is provided in a semiconductor package

PK42. Lands 112a and 112c are respectively formed on both faces of the carrier substrate 111. Internal wiring lines 112b are formed in the carrier substrate 111.

Further, electrode pads 114a to 114c are provided on the semiconductor chips 113a to 113c. Insulating films 115a to 115c are respectively provided in the semiconductor chips 113a to 113c so that the electrode pads 114a to 114c are exposed. Through holes 116a to 116c are respectively formed in the semiconductor chips 113a to 113c so as to correspond to the positions of the electrode pads 114a to 114c. Through electrodes 119a to 119c are respectively formed in the through holes 116a to 116c via insulating films 117a to 117c and conductive films 118a to 118c. The semiconductor chips 113a to 113c in which the through electrodes 119a to 119c are formed are stacked via the through electrodes 119a to 119c. Resin 120a and 120b is implanted into gaps among the semiconductor chips 113a to 113c.

[0056]

Further, protruding electrodes 121 for flip-chip mounting the structure in which the semiconductor chips 113a to 113c are stacked are provided on the through electrodes 119a formed in the semiconductor chip 113a. The protruding electrodes 121 are bonded to the lands 112c provided on the carrier substrate 111. The surface of the semiconductor chip 113a mounted on the carrier substrate 111 is sealed with a sealing resin 122. The structure in which the semiconductor chips 113a to 113c are stacked is mounted on the carrier substrate 111.

[0057]

Further, protruding electrodes 123 for mounting the carrier substrate 111 on the carrier substrate 101 are provided on the lands 112a provided on the reverse face of the carrier substrate 111 so that the carrier substrate 111 is provided above the semiconductor chip 103 so as to be separated from the semiconductor chip 103.

The protruding electrodes 123 are arranged so as to avoid the region on which the semiconductor chip 103 is mounted. For example, the protruding electrodes 123 may be arranged around a peripheral region of the reverse face of the carrier substrate 111. The carrier substrate 111 is mounted on the carrier substrate 101 in a state where the reverse face of the semiconductor chip 103 is exposed by bonding the protruding electrodes 123 to the lands 102c provided on the carrier substrate 101.

[0058]

Thus, it is possible to flip-chip mount the structure in which the semiconductor chips 113a to 113c are stacked on the semiconductor chip 103 in a state where the reverse face of the semiconductor chip 103 is exposed without interposing the carrier substrate between the structure in which the semiconductor chips 111a to 111c are stacked and the semiconductor chip 103. Therefore, it is possible to allow for proper heat dissipation from the semiconductor chip 103 while suppressing an increase in the height when the semiconductor chips 113a to 113c are stacked and thereby to stack the semiconductor chips 113a to 113c, which may be different from the semiconductor chip 103, while suppressing the deterioration of the reliability of the three-dimensionally mounted semiconductor chips 103 and 113a to 113c.

[0059]

For example, an Au bump, a Cu bump and an Ni bump coated with solder, or solder balls may be used as the protruding electrodes 104, 106, 121, and 123. A method of mounting the three-layer structure of the semiconductor chips 113a to 113c on the carrier substrate 111 is described in the above-mentioned embodiment. However, the structure in which the semiconductor chips are stacked, which is mounted on the carrier substrate 111, may consist of two, four or more layers.

[0060]

Fig. 6 is a sectional view illustrating the structure of a semiconductor device according to a sixth embodiment of the present invention. According to the sixth embodiment, a W-CSP (a wafer level chip size package) is three-dimensionally mounted on a carrier substrate 201 on which a semiconductor chip 203 is flip-chip mounted.

In Fig. 6, the carrier substrate 201 is provided in a semiconductor package PK51. Lands 202a and 202c are respectively formed on both faces of the carrier substrate 201. Internal wiring lines 202b are formed in the carrier substrate 201. The semiconductor chip 203 is flip-chip mounted on the carrier substrate 201 so that the reverse face of the semiconductor chip 203 is exposed. Protruding electrodes 204 for flip-chip mounting the semiconductor chip 203 are provided on the semiconductor chip 203. The protruding electrodes 204 provided on the semiconductor chip 203 are bonded to the lands 202c via an anisotropic conductive film 205 by ACF bonding. Protruding electrodes 206 for mounting the carrier substrate 201 on a mother substrate are provided on the lands 202a on the reverse face of the carrier substrate 201.

[0061]

On the other hand, a semiconductor chip 211 is provided in a semiconductor package PK52. Electrode pads 212 are provided on the semiconductor chip 211. An insulating film 213 is provided so as to expose the electrode pads 212. A stress-relieving layer 214 is formed on the semiconductor chip 211 so that the electrode pads 212 are exposed. A re-arrangement wiring line 215 extending on the stress-relieving layer 214 is formed on the electrode pads 212. A solder resist film 216 is formed on the re-arrangement wiring line 215. Apertures 217 for exposing the re-arrangement wiring line 215 on the stress-relieving layer 214 are formed in the solder resist film 216. Protruding electrodes 218 for mounting the semiconductor chip 211 face down on the carrier substrate 201 are provided on the re-arrangement wiring line 215 exposed through the

apertures 217 so that the semiconductor package PK52 is provided above the semiconductor chip 203 so as to be separated from the semiconductor chip 203.

[0062]

The protruding electrodes 218 are arranged so as to avoid the region on which the semiconductor chip 203 is mounted, for example, around a peripheral region of the reverse face of the semiconductor chip 211. The semiconductor package PK52 is mounted on the carrier substrate 201 in a state where the protruding electrodes 218 are bonded to the lands 202c provided on the carrier substrate 201 thereby to expose the reverse face of the semiconductor chip 203.

[0063]

Thus, it is possible to stack the W-CSP on the carrier substrate 201 on which the semiconductor chip 203 is flip-chip mounted. Therefore, even when the kinds or the sizes of the semiconductor chips 203 and 211 vary, it is possible to three-dimensionally mount the semiconductor chip 211 on the semiconductor chip 203 in a state where the reverse face of the semiconductor chip 203 is exposed without interposing the carrier substrate between the semiconductor chips 203 and 211. As a result, it is possible to allow for proper heat dissipation from the semiconductor chip 203 while suppressing an increase in the height when the semiconductor chips 203 and 211 are stacked and thereby to save space when the semiconductor chips 203 and 211 are mounted while suppressing the deterioration of the reliability of the three-dimensionally mounted semiconductor chips 203 and 211.

[0064]

When the semiconductor package PK52 is mounted on the carrier substrate 201, pressure welding such as ACF bonding or NCF bonding may be used. Metal joining such as soldering or alloy joining may be used. For example, an Au bump, a Cu bump and an

Ni bump coated with solder, and solder balls may be used as the protruding electrodes 204, 206, and 218. A method of mounting the semiconductor package PK52 on one semiconductor chip 203 flip-chip mounted on the carrier substrate 201 is described in the above-mentioned embodiment. However, the semiconductor package PK52 may also be mounted on a plurality of semiconductor chips flip-chip mounted on the carrier substrate 201.

[0065]

Moreover, the above-mentioned semiconductor devices and electronic devices can be applied to electronic apparatuses such as liquid crystal displays, mobile telephones, portable information terminals, video cameras, digital cameras, and mini disc (MD) players thereby to miniaturize and lighten the electronic apparatuses and to improve the reliability of the electronic apparatuses.

Further, a method of mounting the semiconductor chips or the semiconductor packages is described in the above-mentioned embodiment. However, the present invention is not necessarily limited to this method of mounting semiconductor chips or semiconductor packages. For example, ceramic elements such as surface acoustic wave (SAW) elements, optical elements such as optical modulators and optical switches, and various sensors such as magnetic sensors and biosensors may be mounted.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a sectional view illustrating the structure of a semiconductor device according to a first embodiment.

[Fig. 2]

Fig. 2 is a sectional view illustrating the structure of a semiconductor device according to a second embodiment.

[Fig. 3]

Fig. 3 is a sectional view illustrating a semiconductor device according to a third embodiment.

[Fig. 4]

Fig. 4 is a sectional view illustrating a method of manufacturing a semiconductor device according to a fourth embodiment.

[Fig. 5]

Fig. 5 is a sectional view illustrating a method of manufacturing a semiconductor device according to a fifth embodiment.

[Fig. 6]

Fig. 6 is a sectional view illustrating the structure of a semiconductor device according to a sixth embodiment.

[Reference Numerals]

21, 31, 41, 51, 61, 61a to 61c, 71, 81, 101, 111, 201: CARRIER SUBSTRATE

22a, 22c, 32a, 32c, 42a, 42c, 52a, 52c, 72a, 72b, 82, 102a, 102c, 112a, 112c, 202a, 202c: LAND

22b, 32b, 42b, 52b, 102b, 112b, 202b: INTERNAL WIRING LINE

23, 33a, 33b, 43, 53a, 53b, 62a to 62c, 73, 103, 113a to 113c, 203, 211: SEMICONDUCTOR CHIP

24, 26, 36, 44, 46, 55a, 56, 65a to 65c, 74, 77, 83, 104, 121, 123, 206, 218: PROTRUDING ELECTRODE

25, 45, 54a, 75, 105, 205: ANISOTROPIC CONDUCTIVE FILM

34a, 34b, 54b: ADHESION LAYER

15, 35a, 35b, 55b, 63a to 63c: CONDUCTIVE WIRE

37, 57, 64, 64a to 64c, 84, 120a, 120b, 122: SEALING RESIN

76: FLUX

114a to 114c and 212: ELECTRODE PAD

115a to 115c, 117a to 117c, 213: INSULATING FILM

116a to 116c: THROUGH HOLE

118a to 118c: CONDUCTIVE FILM

119a to 119c: THROUGH ELECTRODE

214: STRESS-RELIEVING LAYER

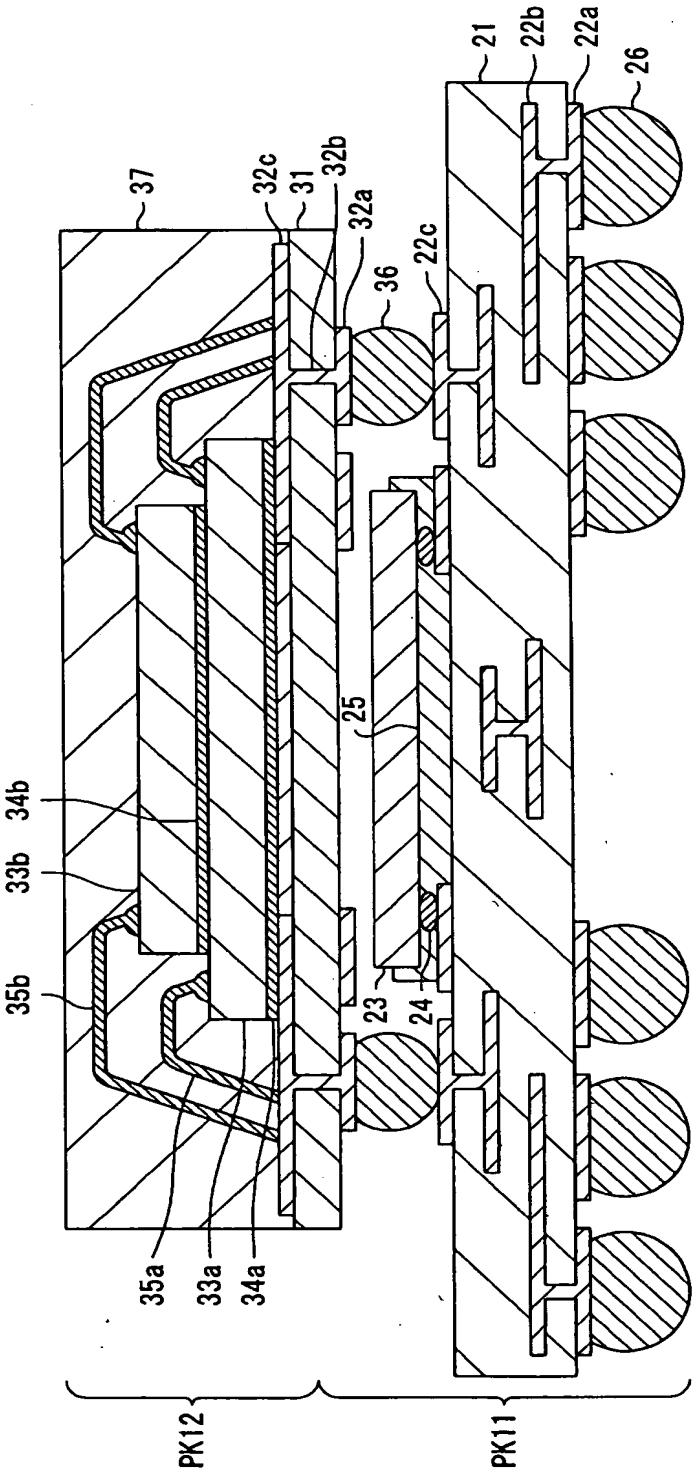
215: RE-ARRANGEMENT WIRING LINE

216: SOLDER RESIST LAYER

217: APERTURE

PK11, PK12, PK21, PK22, PK31, PK32, PK41, PK42, PK51, PK52: SEMICONDUCTOR PACKAGE

FIG.1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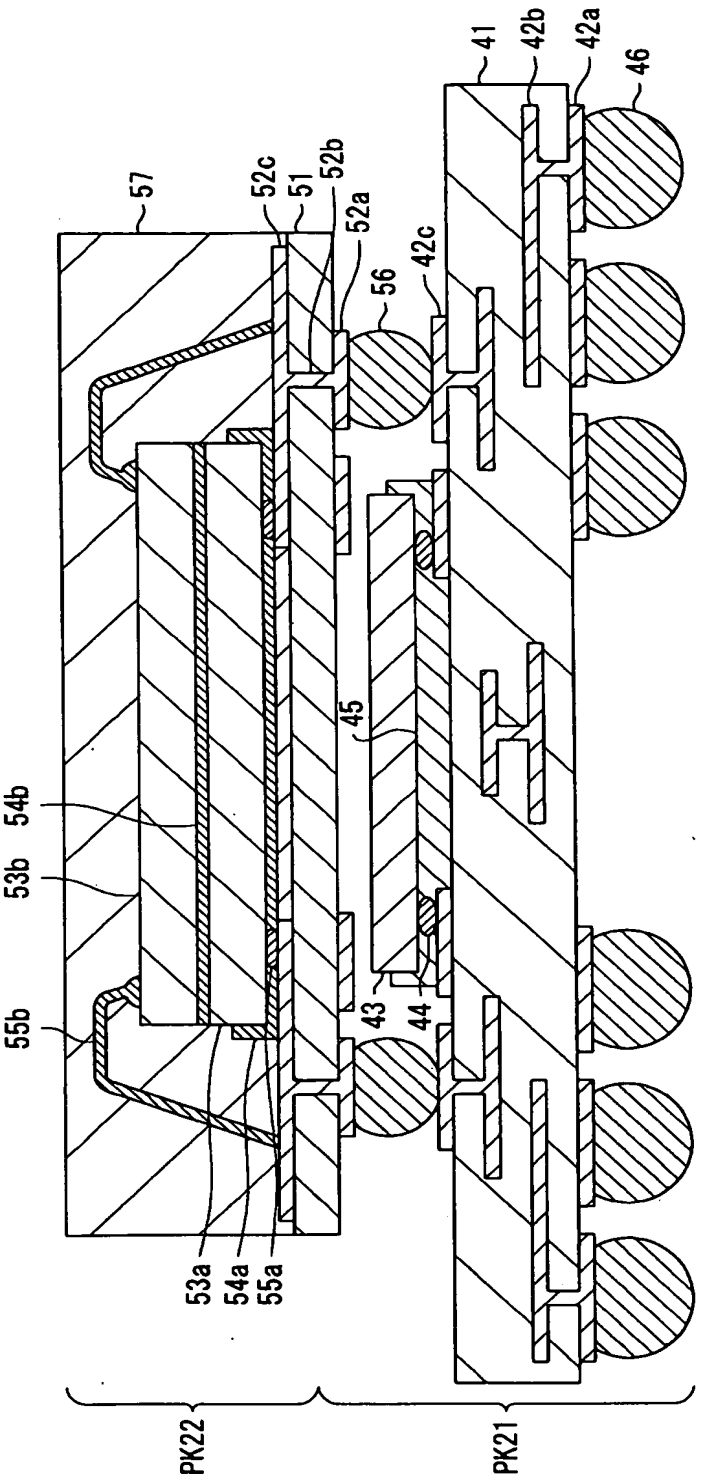
32b
32a
36
22c
21
22b
22a
26
25
34b
33b
35b
23
24
35a
33a
34a
PK12
PK11

FIG.2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52b
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56
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54b
53b
55b
43
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53a
54a
55a
PK22
PK21

FIG.3A

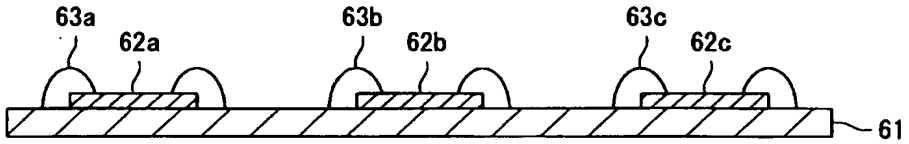


FIG.3B

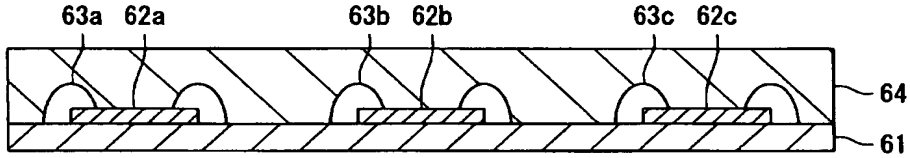


FIG.3C

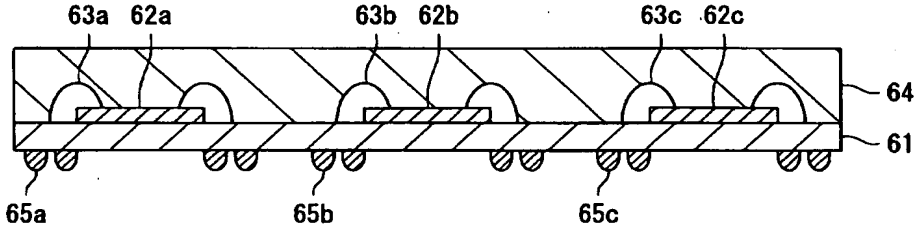


FIG.3D

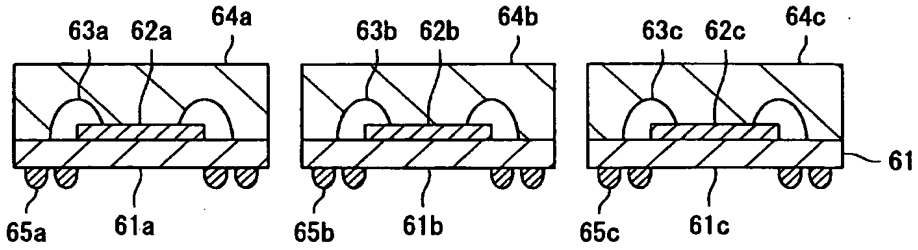


FIG.4A

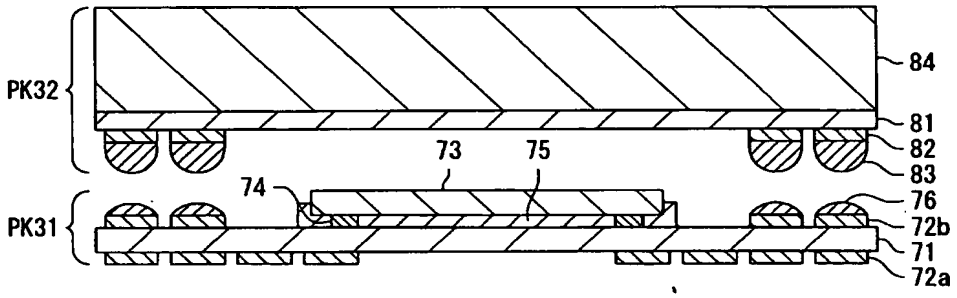


FIG.4B

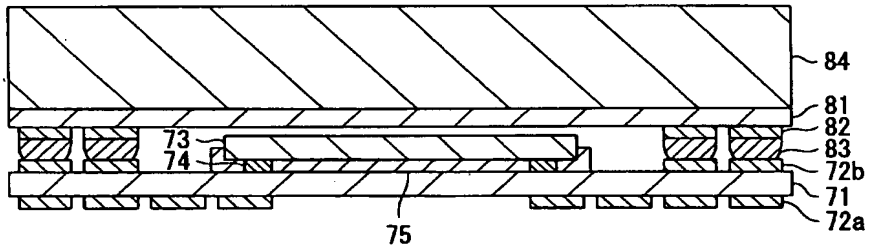


FIG.4C

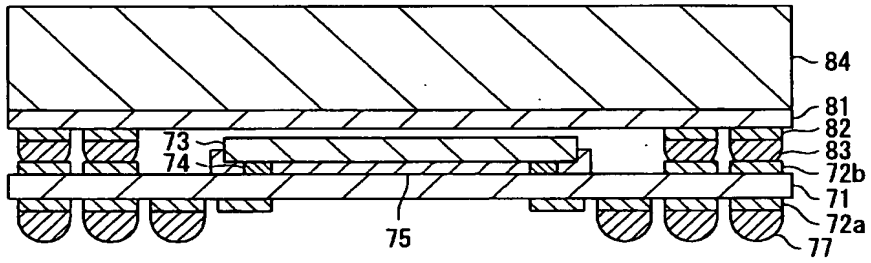
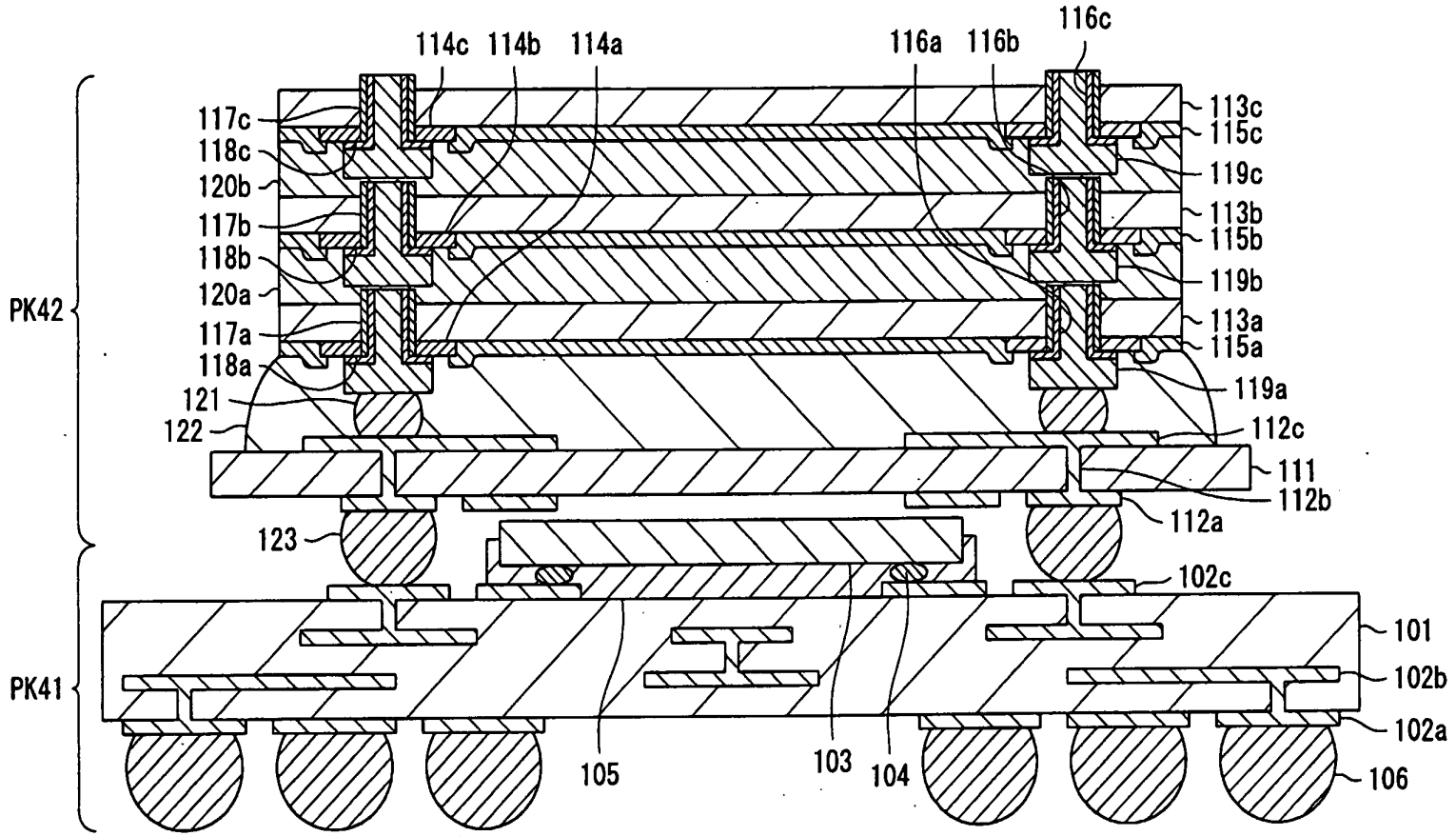


FIG.5


PK42
PK41
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114b
114a
116a
116b
116c
117c
118c
120b
117b
118b
120a
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121
122
123
113c
115c
119c
113b
115b
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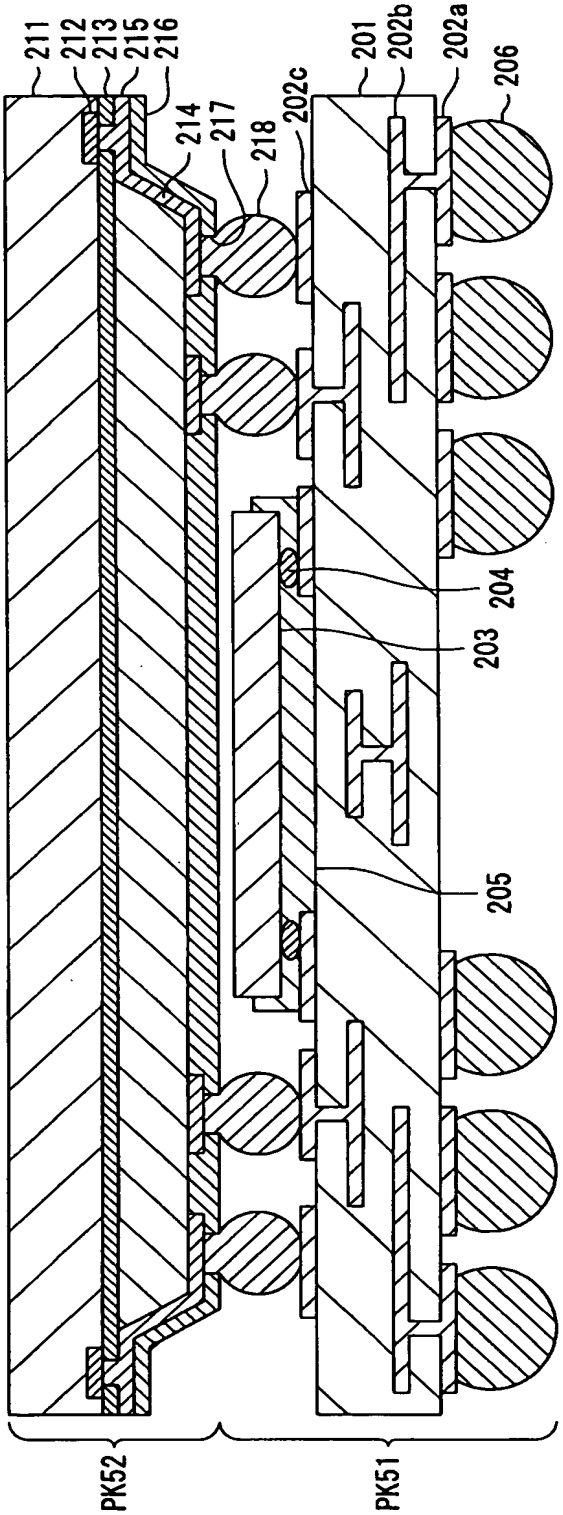
102b
102a
105
103
104
106

FIG.6


211
212
213
215
216
214
217
218
202c
201
202b
202a
206
204
203
205
PK52
PK51

[Name of Document] ABSTRACT

[Abstract]

[Object] To realize a structure in which different kinds of chips are three-dimensionally mounted while allowing for proper heat dissipation.

[Solving Means] A semiconductor package PK12 in which stacked semiconductor chips 33a and 33b are wire-connected is stacked on a semiconductor package PK11 in which a semiconductor chip 23 is mounted by anisotropic conductive film (ACF) bonding. A carrier substrate 31 is mounted on a carrier substrate 21 in a state where the reverse face of the semiconductor chip 23 is exposed.

[Selected Figure] Fig. 1